APPLICATION NOTE

ABSTRACT
The SA8028 frequency synthesizer is targeted for mobile radio systems where either single or multiple standards will be deployed and fast switching times and low phase noise performance is crucial to meeting system requirements. The SA8028 offers low voltage, ultra-low phase noise, and $\Sigma - \Delta$ fractional-N technology that provides ultra-fine frequency resolution.

AN10140

2.5 GHz $\Sigma - \Delta$ fractional-N/ 760 MHz IF integer frequency synthesizer

Robbert Emery

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PHILIPS

2.5 GHz Σ–Δ Fractional-N RF / 760 MHz Integer IF Synthesizer

AN10140

INTRODUCTION TO THE SA8028

1. General Description

The SA8028 BiCMOS synthesizer integrates programmable dividers, charge pumps and phase comparators to implement phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer has fully programmable main (RF), auxiliary (IF) and reference dividers. All divider values are supplied via a 3-wire serial programming bus. The RF loop operates at VCO input frequencies up to 2.5 GHz and includes a programmable, integer, divider with values from 33 to 509 and a programmable 2nd order sigma-delta modulator to achieve fractional division. The frequency resolution is 1/8388608 of the reference frequency. There are 22 programmable bits (23 bits internal) for the fractional calculator. The RF phase comparator operates up to 30 MHz; there is no reference divider for the RF loop.

The IF loop operates at VCO input frequencies up to 760 MHz and includes a reference divider and a divider in the feedback path.

Separate power and ground pins are provided to the charge pumps and digital circuits. V_{DDCP} must be greater than or equal to V_{DD}. The ground pins should be externally connected to prevent large currents from flowing across the die and causing damage.

The charge pump current (phase detector gain) is programmable, while I_{SET} is determined by an external resistance at the R_{SET} pin (refer to the datasheet). The phase/frequency detector charge pump outputs allow for implementing a passive loop filter.

1.1. Functional Block Description

There are six fundamental functional blocks for programmable PLLs. Figure 1 illustrates the location of these blocks with respect to the overall loop, whereas Figure 2 illustrates a general block diagram of the SA8028 frequency synthesizer, as an IC.

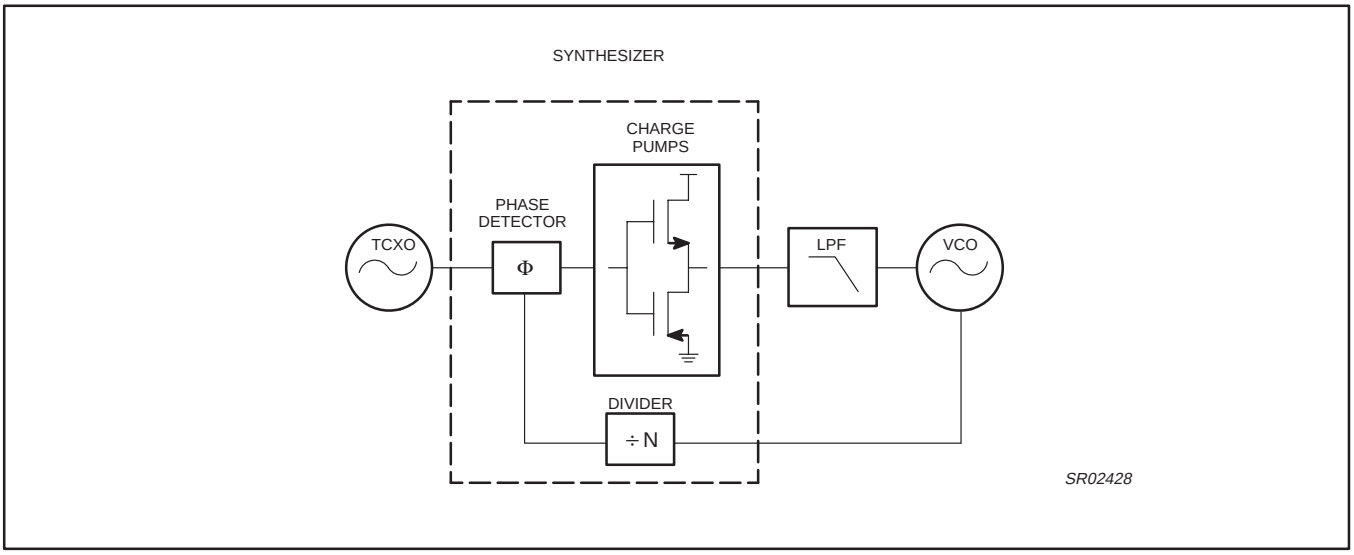


Figure 1. Fundamental PLL Block Diagram.

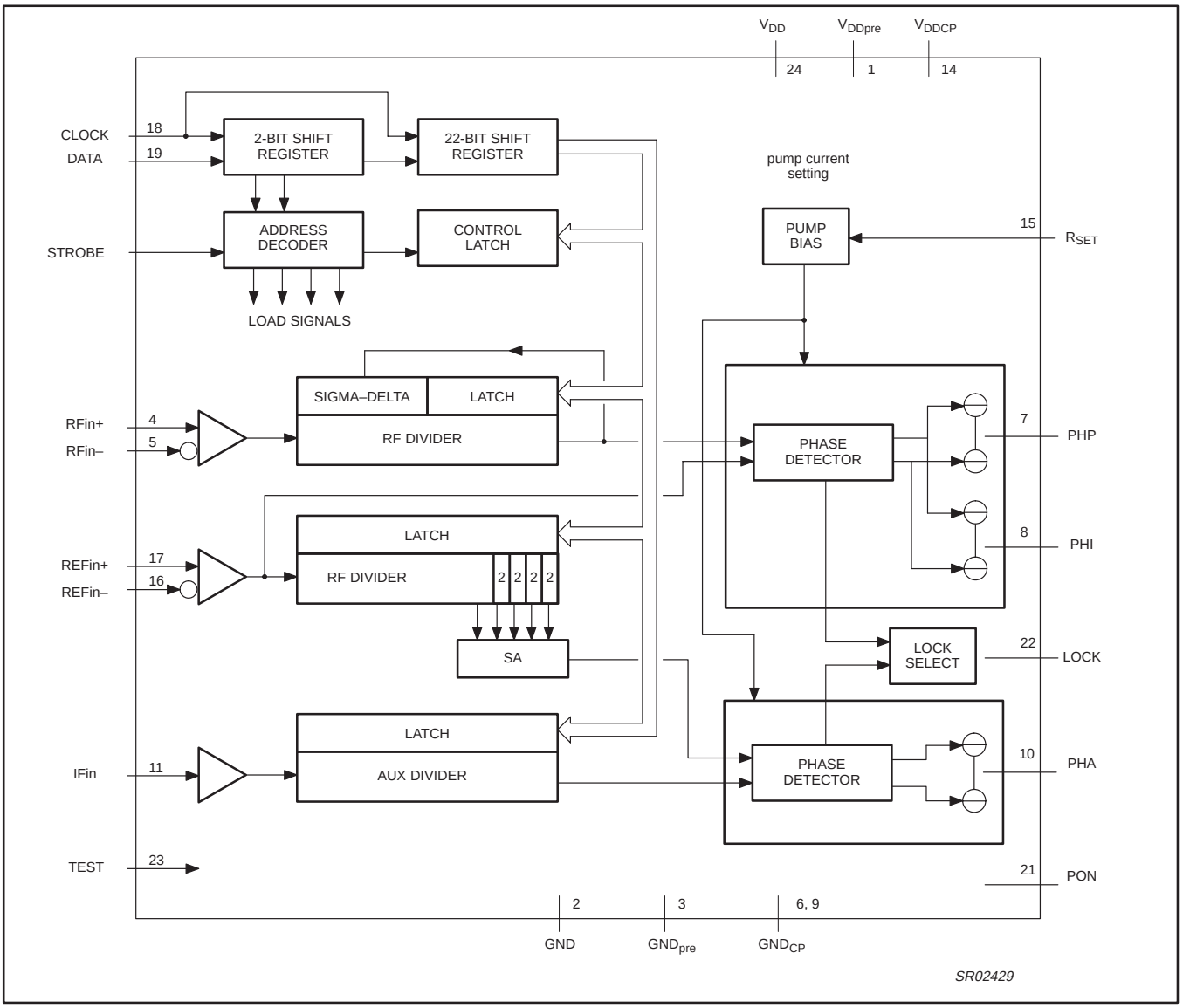
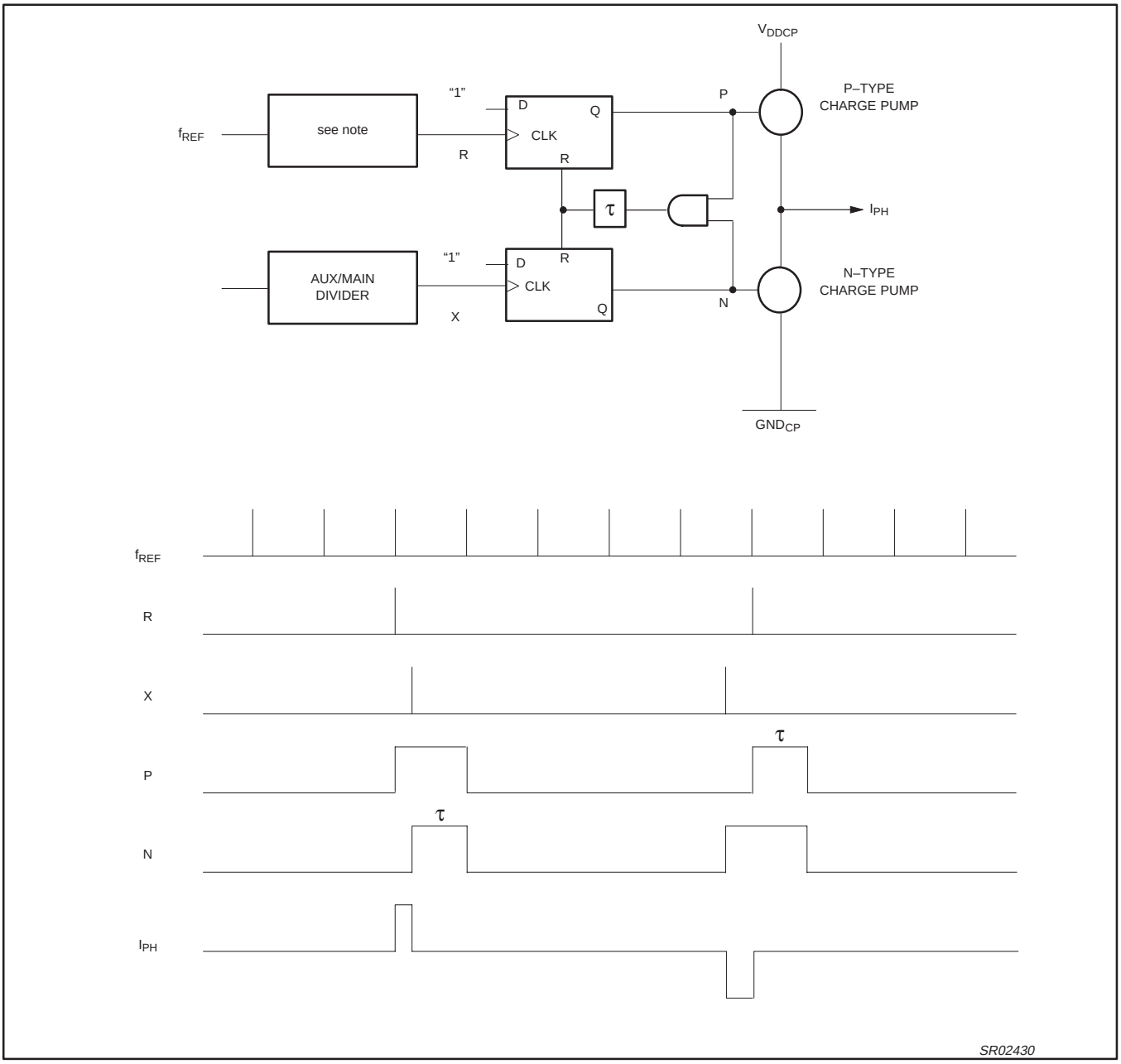


Figure 2. HBCC24 Block Diagram.

1.1.1. Frequency Phase Detector (FPD)

The RF frequency phase detector drives the charge pumps on the PHP and PHI pins, while the IF phase detector drives the charge pump on the PHA pin. The FPD is a simple logic circuit that compares pulses from two sources (e.g., the reference frequency and the output from the RF divider). Figure 3 shows the operation of the FPD and the resultant output of the charge pumps.

The f_{REF} signal is a pulse replication of the reference source. The 'R' and 'X' signals are a closer look at the signals exercising the FPD. The 'R' signal representing the reference, typically a signal generated from a crystal, and the 'X' signal representing the output from the RF or the IF dividers. Notice when the 'R' pulse leads the 'X' pulse, the 'P' signal, from the P-pump, goes high until the 'X' pulse, plus some time delay (τ), resets the flip-flop. When the 'X' pulse leads the 'R' pulse, the 'N' signal, from the N-pump, goes low until the 'R' pulse, plus some time delay (τ), resets the flip-flop. τ is a time delay called "backlash" which eliminates "cycle skipping" by forcing both the P-pump and the N-pump on for a minimal amount of time during each FPD cycle. Cycle skipping occurs when one or more FPD cycle(s) extends beyond $\frac{1}{f_{FPD}}$, where f_{FPD} is the phase detector frequency. Accordingly, the net charge pump output current is represented by the I_{PH} signal.



Note: For the main synthesizer, the output of the reference input buffer is routed directly (not divided) to the input of the main phase detector. Whereas for the auxiliary synthesizer, the reference input to the auxiliary phase detector is the output from the reference divider.

τ is a delay that fixes the minimum allowable charge-pump activity time.

Figure 3. Phase Detector Structure with Timing.

Because the frequency/phase detector is digital and thermally dissipates current, it is a source of spectral noise. Its contribution is calculated by:

$$10 \times \log(f_{FPD}) \quad (1)$$

where f_{FPD} is the phase comparator frequency (in the case of the RF loop, the phase comparator frequency is the same as the reference frequency; there is no reference divider for the RF loop). The SA8028 FPD operates at frequencies up to 30 MHz. Increasing the FPD frequency reduces the number of divide stages in the feedback path. At first, this may seem to be undesirable. However, the SA8028 RF loop can achieve any frequency step (channel spacing) with an accuracy of less than +/–4Hz.

The difference in phase noise contribution from one FPD frequency to another FPD frequency can be calculated by:

$$\Delta L(f)_{FPD} = \left|10 \times \log\left(f_{FPD2}\right) - 10 \times \log\left(f_{FPD}\right)\right| \quad (2)$$

$$L(f)_{FPD} \equiv \textit{FPD phase noise} \left(\frac{dBc}{Hz}\right)$$

The benefit of increasing the FPD frequency is a reduction in the divider stages, N, of the feedback path in the PLL. This will reduce the synthesizer noise generated by the dividers. Section 1.1.3 describes the divider noise in more detail.

1.1.2. Charge Pumps

Both the RF and IF charge pump current values are determined by the current generated at the R_{SET} pin.[1]

$$Iset = \frac{Vset}{Rset} \quad (3)$$

The current gain can be further programmed by the CP0, CP1 bits in the C-word, as shown in Table 1.

Table 1. RF and IF charge pump currents

CP1[2]	CP0	I_{PHA}	I_{PHP}	$I_{PHP–SU}$[3]	I_{PHI}
0	0	1.5xI_{SET}	3xI_{SET}	15xI_{SET}	36xI_{SET}
0	1	0.5xI_{SET}	1xI_{SET}	5xI_{SET}	12xI_{SET}
1	0	1.5xI_{SET}	3xI_{SET}	15xI_{SET}	0
1	1	0.5xI_{SET}	1xI_{SET}	5xI_{SET}	0

NOTES:
1. $I_{SET} = V_{SET}/R_{SET}$: bias current for charge pumps.
2. CP1 is used to disable the PHI pump.
3. $I_{PHP–SU}$ is the total current at pin PHP during speed up condition.

The programmable charge pump gains provide some adaptability to the loop filter bandwidth $\left(BW \propto \sqrt{K_\phi}\right)$ (refer to Section 1.1.3 for more discussion on this feature). This feature is useful for multi-standard applications (e.g., CDMA switching speed vs. AMPS spurious rejection).

Example: A dual mode system (CDMA & AMPS) will require fast switching times for CDMA and adequate spurious rejection for AMPS. Therefore, the loop filter and bandwidth will be optimized for switching time and integrated phase error for CDMA using the 3xIset mode, CP0 = 0, while the loop bandwidth will be reduced by $\sqrt{3}$ when CP0 is set to 1. This may raise questions about the transient and peaking in either or both the CDMA and AMPS modes. To help answer this question, keep in mind that there is no strict switching requirement for AMPS, 3 to 10 mS is easily achieved using the speed-up mode.

The PHP and PHA charge pumps are used for normal operation (steady state) of the PLL circuit. PHP_SU and PHI should only be used during large frequency steps (dynamic state) to aid in acquiring the desired signal much more rapidly (charge pump speed-up mode is described in more details in Section 1.1.2.1). The charge pump output must be integrated to tune the VCO. This is done by the recommended loop filter shown in Figure 4.

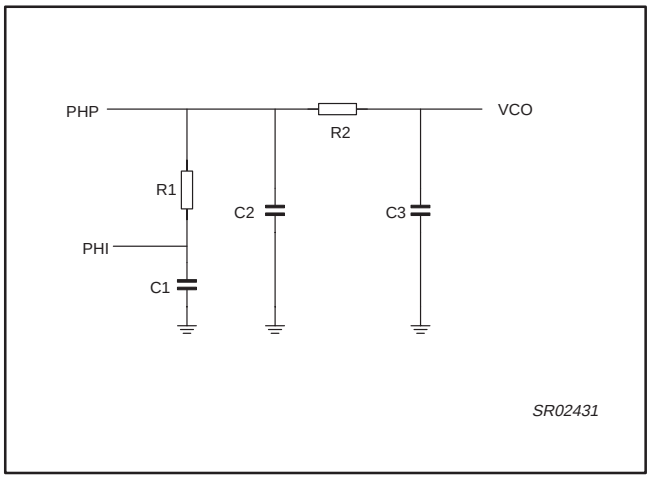


Figure 4. Recommended loop filter configuration.

1.1.2.1. Charge Pump Speed-up Mode

The RF charge pumps, PHP and PHI, will enter speed-up mode when the STROBE pulse following the A-word goes ‘high’. The charge pumps will exit speed-up mode on the next falling edge of the STROBE pulse. There is no speed-up mode for the IF charge pump.

The charge pump, by default, will automatically go into speed-up mode (which can deliver up to 15*I_{SET} for PHP_SU, and 36*I_{SET} for PHI), based on the strobe pulse width following the A-word. This action pre-charges the loop filter, thus reducing switching speed (capacitance charging/discharging times) for large tuning voltage steps (i.e., large frequency steps).

The duration of speed-up mode is determined by the width of the strobe pulse following the A-word. An external data processing unit controls the width of the strobe pulse (e.g. × number of clock cycles). The recommended optimal strobe width (T_{STROBE}) is equal to the total loop filter capacitance charge time (T_{ch}) from VCO control voltage state 1 to state 2.

$$T_{STROBE} = T_{ch} = \frac{C_{TOTAL}}{I_{AVERAGE}} \times \Delta V \quad (4)$$

The average current from the total current produced by the charge pump(s) can be determined by:

$$I_{AVERAGE} = 0.3 \times |GAIN| \times I_{set}$$

The one third takes into account ‘backlash’ and charge pump, high gain, mismatch effects for the loop filter configuration shown in Figure 4 for PHP_SU = 15*I_{SET} and PHI = 36*I_{SET}. The strobe width must not exceed this charge time.

1. $I_{SET} = V_{SET}/R_{SET}$: bias current for charge pumps.

In addition, charge pumps will stay in speed-up mode continuously while Tspu = 1 (in D-word). The speed-up mode can also be disabled by programming $T_{dis\text{-}spu}$ = 1 (in D-word). It is important to note that the noise introduced by the charge pumps increases with higher gain modes. Thus, it is recommended to use the 3xIset and 1xIset modes in normal operation (steady state).

1.1.3. RF (Main) Divider

The differential RFin inputs drive a pre-amplifier to provide a clock to the first divider stage. For single ended operation, the signal should be AC-coupled to one of the inputs (typically RFin+) while the other one is AC-grounded (typically RFin–). The pre-amplifier has high input impedance, dominated by pin and pad capacitance. The divider is fully programmable with a bipolar prescaler.

During each RF divider cycle, one divider output pulse is generated, which drives the phase comparator. The sigma-delta modulator, also driven by this pulse, is programmed to achieve the desired frequency step and has an effective resolution of 22 bits, $f_{ref}/2^{22}$. Internally, the modulator works with 23 fractional bits Kn<22:0>, but the LSB (bit K0) is set to '1' internally to avoid limit cycles (cycles of less than maximum length). Cycles of maximum length provide the highest degree of randomness for the modulation calculator. Therefore, 22 bits (Kn<22:1>) are available for external programming.

Under these conditions (2^{nd} order modulator, 23 fractional bits, K0 = '1') all possible sigma-delta sequences are 2*(2^23) divider cycles long which is the maximum length. The noise-shaping characteristic is +20 dB/dec for offset frequencies up to approximately fcomp/5, which needs to be cancelled by a filter of sufficient high order. The output of the sigma-delta modulator is 2 bits, which are added to the integer RF division ratio N, such that the momentary division ratio ranges from (N–1) to (N+2) in steps of 1.

Programming of the RF divider, to obtain the desired VCO output frequency, is done by programming the B-word, followed by the A-word. The integer divide bits, N<8:0>, are in the B-word and the fractional divider bits Kn<22:1> are in the A-word. Allowable integer division ratios are outlined in Table 2, while Table 3 shows the possible Kn values that can be programmed into the A-word. The calculation of the desired VCO output frequency can be accomplished by using equation (5).

$$f_{VCO} = f_{ref}\left(N + \frac{2 \times Kn + 1}{2^{23}}\right) \quad (5)$$

where f_{ref} is the reference frequency at the REFin+ (REFin–) input pin.

Example: Determine the expected VCO frequency with an input reference frequency of 19.68 MHz, an N value of 106 and a Kn value of 17.

F_{VCO} = 19.68 MHz*(106 + (2x17+1)/2^23) = 2086.080082 MHz.

Example: Determine the Kn value required for generating a VCO frequency of 2100 MHz with a reference frequency of 19.68 MHz.

$$Kn = \left\lceil \frac{\left[\left(\frac{fVCO}{fref} - N\right) \times 2^{23}\right]}{2} - 1 \right\rceil, \text{ for } 0 < \frac{fVCO}{fref} - N < 1$$

$$Kn = 0, \text{ for } \frac{fVCO}{fref} - N = 0$$

$$Kn = \left\lceil \frac{\left[\left(\frac{2100MHz}{19.68MHz} - 106\right) \times 2^{23}\right]}{2} - 1 \right\rceil = 2966702$$

Note: $\lceil\ \rceil$ means round up if value is > 0.5.

Table 2. Allowable integer values (N) for the RF divider

8	7	6	5	4	3	2	1	0	<B:N>
0	0	0	1	0	0	0	0	1	**33**
0	0	0	1	0	0	0	1	0	**34**
0	0	0	1	0	0	0	1	1	**35**
–	–	–	–	–	–	–	–	–	…
1	1	1	1	1	1	1	0	1	**509**

Table 3. Kn Values for the Fractional Divider represented as bits A<0:21>

A 21	A 20	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8	A 7	A 6	A 5	A 4	A 3	A 2	A 1	A 0	Kn
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	…
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	4194302
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	4194303

The noise contribution from the divider block in the feedback path is:

$$20 \times \log(N) \quad (6)$$

Thus, the difference in phase noise contribution from one N value to another N value can be calculated by:

$$\Delta L(f)_{divider} = |20 \times \log(N_2) - 20 \times \log(N_1)| \quad (7)$$

1.1.4. Loop Filter

Figure 4 in Section 1.1.2 illustrates the recommended configuration of the passive loop filter.

When designing the loop filter, use only the steady state conditions for the following equations. There are many parameters to consider when designing the loop filter. Equation (8) is a starting point for a good, filter design process.

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_\phi \times K_{VCO}}{N \times C_1}} \quad (8)$$

$f_n \equiv$ Loop filter natural frequency (Hz)

$$K_\phi \equiv FPDgain \equiv \left[\frac{\frac{V_{SET}}{R_{SET}} \times \text{charge pump gain}}{2\pi}\right]\left(\frac{A}{\text{radian}}\right)$$

$$K_{VCO} \equiv \text{VCO gain}\left(\frac{Hz}{V}\right) \text{ or } 2\pi \times \text{VCO gain}\left(\frac{\text{radian}}{V}\right)$$

$N \equiv$ *Integer divider value*

In determining the loop filter's corner frequency, the VCO phase noise characteristics must be known. The loop filter natural frequencies is typically chosen where $L(f)_{VCO}$ and $L(f)_{SYNTH}$ intersect.

$$L(f)_{VCO} \equiv VCO \text{ phase noise}\left(\frac{dBc}{Hz}\right)$$

$$L(f)_{SYNTH}\left(\frac{dBc}{Hz}\right) \equiv \left(-209 + L(f)_{FPD} + L(f)_{divider}\right)\left(\frac{dBc}{Hz}\right)$$

The derivation of the –209 dBc/Hz is described in more detail in Section 2.

Once this frequency is known, C1 is calculated by re-arranging equation (8) as follows:

$$C_1 = \frac{K_\phi \times K_{VCO}}{N(2\pi fn)}$$

The N value to choose is preferably from the center of the VCO tuning range. Once C1 is calculated, R1 is determined by:

$$R_1 = 2 \times \zeta\left(\sqrt{\frac{N}{K\phi \times K_{VCO} \times C_1}}\right) \quad (9)$$

$\zeta \equiv$ damping factor

The damping factor is typically chosen as 0.707 for best phase margin. However, the frequency switching time can be reduced by increasing this value closer to 1.0 for better in-band, integrated phase noise.

C1 and R1 are the minimum requirements for the filter. However, a single pole filter may not be enough to meet system requirements. A second pole can be added by simply adding another capacitor using the following 'rule of thumb'.

$$C_2 \leq \frac{C_1}{10}$$

This method assures loop stability. Another method that requires validation for loop stability is

$$f_2 = \frac{1}{2\pi(R_1 \times C_2)} \quad (10)$$

The loop phase margin reduces as f_2 gets closer to f_n. Another 'rule of thumb' for the third pole is

$$f_3 = \frac{1}{2\pi(R_2 \times C_3)} \geq 10 f_N \quad (11)$$

An approximated calculation for frequency switching speed is done with equation 12.

$$tsw = taq + tch \quad (12)$$

$tsw \equiv$ frequency step switching time (sec)

$$taq = \frac{-\ln\left(\delta\sqrt{1-\zeta^2}\right)}{\omega_n \times \zeta} \quad (13)$$

$taq \equiv$ frequency acquisition time (sec)

$$\delta \equiv \text{Residual frequency error tolerance} = \frac{\text{freq. settling error}}{\text{freq. step size}}$$

$$\omega_n \equiv 2\pi f_n \text{ (radians)}$$

$$tch = \frac{C_{TOTAL}}{I_{AVERAGE}} \times \Delta V$$

The loop filter, 3 dB bandwidth as a function of the loop's natural frequency is calculated from equation 14.

$$BW_{3dB} = f_n \times \sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}} \quad (14)$$

$BW_{3dB} \equiv$ 3dB bandwidth of the loop filter

With the above information, and knowledge of the application specifications, an entire passive, third order filter can be designed. Section 2 provides a step by step example of a loop filter design.

1.1.5. IF (AUX), Reference Divider

The reference divider chain consists of a bipolar input buffer followed by a CMOS divider and a 3 bit binary counter (SA register). The IF phase detector's reference input is an integer ratio of the reference frequency. Allowable divide ratios, R, are from 4 to 1023 (B-word bits <21:12>) when the 3 bit binary counter (C-word bits <2:0>) is set to all zeros, SA = 000. The 3 bit SA register determines which of the 5 divider outputs (refer to Table 4) is selected as the IF phase detector's input (see Figure 5).

Table 4. IF Phase comparator Frequency

<C2>	<C1>	<C0>	Divide Ratio	IF Phase comparator Frequency
0	0	0	R	f_{ref} [1]/ R
0	0	1	R * 2	f_{ref} / (R * 2)
0	1	0	R * 4	f_{ref} / (R * 4)
0	1	1	R * 8	f_{ref} / (R * 8)
1	0	0	R * 16	f_{ref} / (R * 16)

NOTE:

1. f_{ref} is the input frequency at the REFin+ (REFin–) pin.

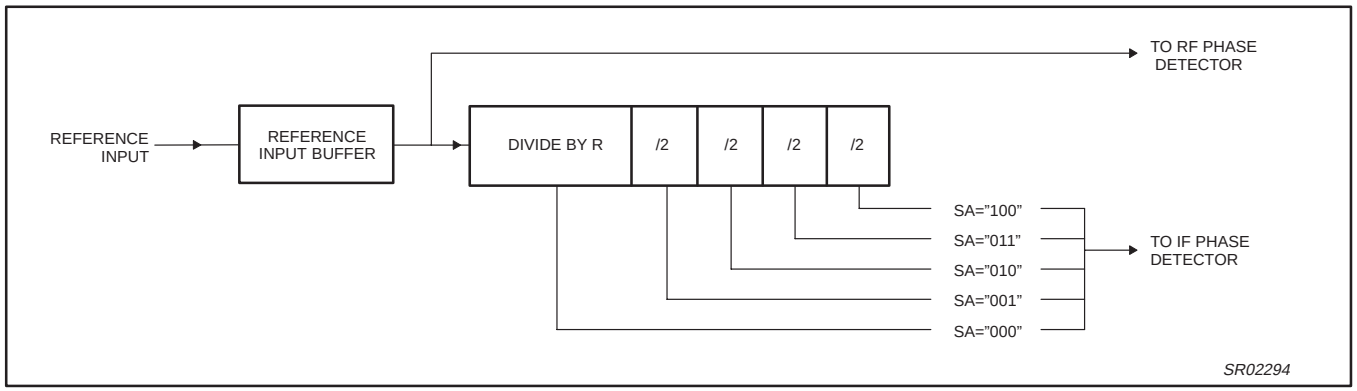


Figure 5. Reference divider.

1.1.6. IF (AUX) Divider

A single ended, high frequency pre-amplifier at the input of the IF divider shapes the IF signal, providing a clock for the first stage of the divider. The pre-amplifier has high input impedance, dominated by pin and pad capacitance. The divider consists of a bipolar pre-scalar followed by a fully programmable CMOS counter. The allowable divide ratios, A, are from 128 to 16383 (‘C word’ bits <21:8>). Table 5 shows all the possible values that can be programmed into the ‘A word’ for the IF divider.

Table 5. Allowable Values (A) for the IF Divider

<21>	<20>	<19>	<18>	<17>	<16>	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	A
0	0	0	0	0	0	1	0	0	0	0	0	0	0	**128**
0	0	0	0	0	0	1	0	0	0	0	0	0	1	**129**
0	0	0	0	0	0	1	0	0	0	0	0	1	0	**130**
–	–	–	–	–	–	–	–	–	–	–	–	–	–	…
1	1	1	1	1	1	1	1	1	1	1	1	1	0	**16382**
1	1	1	1	1	1	1	1	1	1	1	1	1	1	**16383**

1.1.7. Programming Registers

The SA8028 is a programmable frequency synthesizer. The functionality is organized into four main latch banks: the ‘A-word’, the ‘B-word’, the ‘C-word’ and the ‘D-word’. A simple 3-line, bi-directional, serial bus (DATA, CLOCK and STROBE) is used to program the circuit. The clock driver is enabled when the STROBE = 0. On the rising edges of the CLOCK signal, DATA is latched into two temporary shift registers. One 2-bit shift register that holds the latch address and a 22-bit shift register that holds the latch functional information (refer to Figure 2). On the rising edge of the STROBE, the clock is disabled and the data in the shift registers are latched into different working registers, depending on the address bits. In order to fully program the circuit, 3 words must be sent in the following order: C, B, and A. An additional word, the D-word, is primarily for test purposes. All bits in this test word should be set to 0 upon initially applying power for normal operation (refer to the ’D-word register’ section of the data sheet for more information).

The N value of the B-word is stored, but not implemented until after the A-word is loaded to avoid temporarily false N settings while the corresponding fractional ratio Kn is not yet active. When a new fractional ratio is loaded into the A-word, the sigma-delta modulator does not reset, but rather it will start the new fractional sequence from the last state of the previously executed sequence. A typical programming sequence is illustrated in Figure 6 (refer to the datasheet for time requirements). When loading several words in series, the minimum STROBE high time between words must be observed.

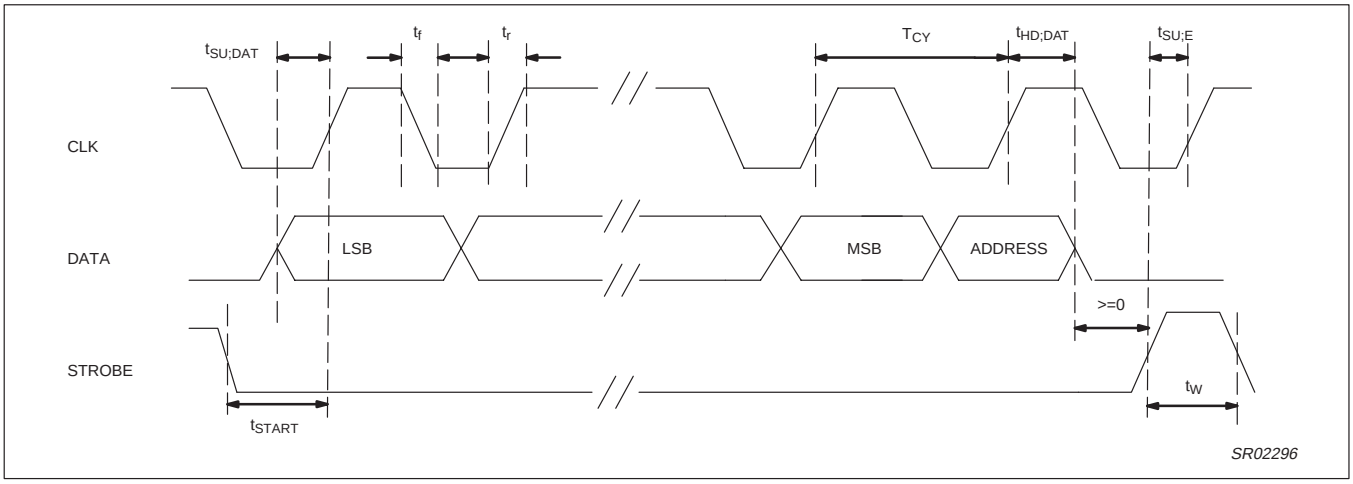


Figure 6. Serial bus "Write" timing diagram.

1.1.7.1. The A-word Register

The A-word register is dedicated for programming the RF loop and the fractional multiplier (the sigma-delta modulator) which has an effective resolution of 22 bits. The modulator works with 23 bits, Kn<22:0>. However, the bit K0 is set to '1' internally to avoid limit cycles (cycles of less than maximum length). This leaves 22 bits (Kn<22:1>) available for external programming. Calculating the desired VCO output frequency can be easily accomplished by using equation (5).

1.1.7.2. The B-word Register

The integer divider bits N<8:0> are in the B-word. Programming the RF divider to obtain the desired VCO output frequency is done by setting the desired bits in the B-word, followed by the A-word. The N value, from equation 5, is simply the integer number of times the desired VCO output frequency can be divided by Fcomp. The allowable N values are from 33 to 509. Note, there is no divider between the REFin+ (REFin–) pin and the FPD for the RF loop. In other words, the frequency at the REFin+ (REFin–) input is the comparison frequency.

The B-word also contains bits that controls the RF (main) and IF (auxiliary) FPD power-down modes. If the chip is programmed while in power-up mode, the loading of the A-word and of the N values of the B-word are synchronized to the RF divider output pulse. The data takes effect internally on the second falling edge of the RF divider output pulse after STROBE has gone high at the end of the A-word. STROBE does not need to be held high until that second falling edge of the RF divider output pulse has occurred. If the chip is programmed while in power-down mode, this synchronization scheme is disabled. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data, even during power-down.

To take advantage of the program register pre-loading capability while the device is in power-down mode, the B-word needs to be sent a second time (i.e. again, after the A-word) with the PD bits now programmed for power-up. If the power-up mode is to be entered by hardware, the PON signal should be toggled only after all the desired bits are set (including C-word, B-word, and A-word) and the STROBE signal has gone high and then low.

When the synthesizer is reactivated after power-down mode, the IF and reference dividers are synchronized to avoid random phase errors on power-up. There is no power-up synchronization between the RF divider and the reference clock. However, after power-up, there is a four-edge delay (i.e. 1.5 cycles) of the reference divider's output clock before the RF phase detector becomes activated. This means the reference divider must be powered up, B<11> = 0, for the RF phase detector to become activated.

Bit B<11> controls the reference divider in the IF path. Setting B<11> to the high state disables the IF reference divider and allows for extra current savings of approximately 200uA. This is not the same as setting bit B<10> to the low state. If it is desired not to use the IF portion of the IC, setting both bits B<10> and B<11> will provide the most savings in current consumption. Conversely, if the IF loop is to be used, bits B<21:12> set the reference divider, which establishes the IF comparison frequency (Fcomp), in conjunction with the optional SA divider (discussed in Section 1.1.5). The IF phase detector's reference input is an integer multiple of the frequency at the input of the REFin+ (REFin–) pin. Allowable divide ratios, R, are from 4 to 1023.

When initially applying or re-applying power to the chip, an internal power-up reset pulse is generated which sets the programming-words to their default values and resets the sigma-delta modulator to its "all–0" state. It is also recommended that the D-word be manually reset to all zeros, following initial power-up, to avoid unknown states.

1.1.7.3. The C-word Register

A 3-bit SA register determines which of the 5 divider outputs (see Table 4) is selected as the IF phase detector's input (see Figure 5).

Bits C<5:4> set the lock detect functionality (refer to Table 6). Again, if it is desired not to use the IF loop, setting bit C<4> to its low state will produce a 'high' at the lock pin when the RF loop is locked.

Table 6. Lock Detect Select

L1	L0	Select
0	0	RF .AND. IF in push/pull mode.
0	1	RF .AND. IF in open drain mode.
1	0	RF only in push/pull mode.
1	1	IF only in push/pull mode.

The PHP and PHI charge pumps are driven by the RF phase detector, whereas the PHA charge pump is driven by the IF phase detector. The current generated at the R_{SET} pin[1] determines both the RF and IF charge pump current values in conjunction with the current gain programmed by the CP0, CP1 bits in the C-word, as shown in Table 1.

The IF (auxiliary) divider is also programmed in the C-word, bits C<21:8>. The allowable divide ratios, A, are from 128 to 16383. The IF divider is an integer divider only. Therefore, the VCO output frequency is an integer multiple of the phase comparator frequency (Fcomp).

1.1.7.4. The D-word Register

The D-word holds factory settings for device functionality tests. It is not intended for normal use. However, some applications may find a few of these functions convenient. Bits D<14:12> control many divider tests. Setting these bits to ”1” will enable a reference buffer output at the LOCK pin. This function can be enabled at the expense of the lock detect pulse. Either the lock detect or the reference buffer can be active at a time. The Tspu = 1 bit will enable the charge pump speed-up mode continuously. On the other hand, the speed-up mode can be disabled by programming $T_{dis–spu}$ = 1. If at any time both bits are set to “1”, $T_{dis–spu}$ take precedence; the speed-up mode will be disabled. It is important to note that the noise contributed by the charge pumps increases with higher gain modes. Thus, it is recommended that the user make use of either the 1xIset of 3xIset modes in normal operation (steady state). Refer to the data sheet for more information on the D-word.

2. Application Design Example

In designing a PLL, there are really only a small hand full of critical parameters to consider (e.g. phase noise, spurious levels, frequency resolution, switching speeds, VCO gain, VCO tuning range and the compliance voltage range from the PFD). In this example, we will consider all the critical parameters for a tri-mode, dual band, IS-2000 mobile phone used in the United States. Therefore, the PLL will have to achieve at least 10 kHz-frequency resolution to comply with both CDMA and AMPS channel spacing requirements. In addition, for this example, a KSS, 19.68 MHz, VC-TCXO-208C have been chosen for the reference signal. Also, the Fujitsu dual band VC-2R8A26-1065/2134 VCO has been chosen for the RF signal source. The next step is to tabulate all the PLL critical parameters for each of these standards.

Table 7. PLL design parameters for dual band tri-mode, U.S. market

Parameters Receive Band	IS-137A	IS-2000 Band Class 0	IS-2000 Band Class 1	Critical requirements (trend)
PLL compliance voltage range (VCO tuning range)	0.6 to Vddcp – 0.7 Volts (0.6 to 2.3 Volts)	0.6 to Vddcp – 0.7 Volts (0.6 to 2.3 Volts)	0.6 to Vddcp – 0.7 Volts (0.6 to 2.3 Volts)	< 2.9 Volts (0.6< V_t < 2.3 Volts)
Frequency range (VCO Gain)	869 to 894 MHz (>11 MHz/V)	869 to 894 MHz (>11 MHz/V)	1930 to 1990 MHz (>26.1 MHz/V)	Dual band VCO
Frequency resolution	30 kHz	30 kHz	50 kHz	10 kHz
Phase noise	–115 dBc/Hz@60 kHz	–115 dBc/Hz@60 kHz –140 dBc/Hz@900 kHz	–115 dBc/Hz@120 kHz –135 dBc/Hz@1250 kHz	–115 dBc/Hz@60 kHz –140 dBc/Hz@900 kHz
Spurious levels	<–65 dBc@60 kHz	<–75 dBc@200 kHz	<–75 dBm@550 kHz	<–65 dBc@60 kHz
Frequency switching time	<2 mS	1 mS	1 mS	(<0.5 mS)

From the above table, phase noise, frequency and tuning ranges are limited strictly by the VCO (the limiting phase noise parameter on the VCO will become clearer later in the example). Hence, the other four items are limited by the integrated synthesizer (divider(s), PFD and charge pumps).

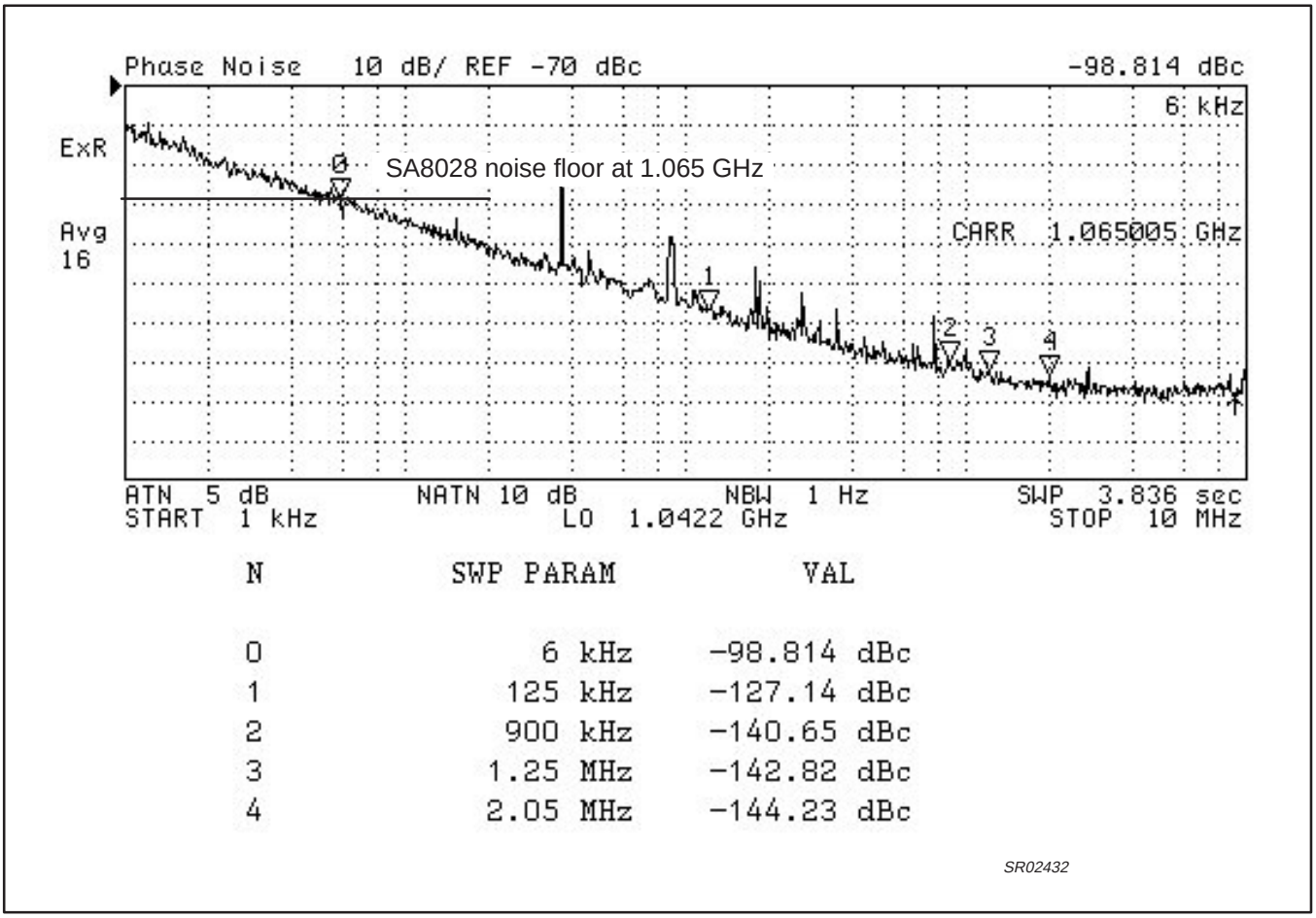


Figure 7. VCO Phase Noise plot for CEL band.

Before putting all the pieces together, a thorough investigation and characterization must be performed on the chosen VCO.

Figure 7 shows that the critical phase noise requirement is met at both 60 kHz and 900 kHz for both the AMPS and CEL-CDMA standards (using the Fujitsu dual band VC-2R8A26-1065/2134 VCO). The phase noise for the US-PCS band is shown in Figure 8. This also supports the use of this VCO for dual band design.

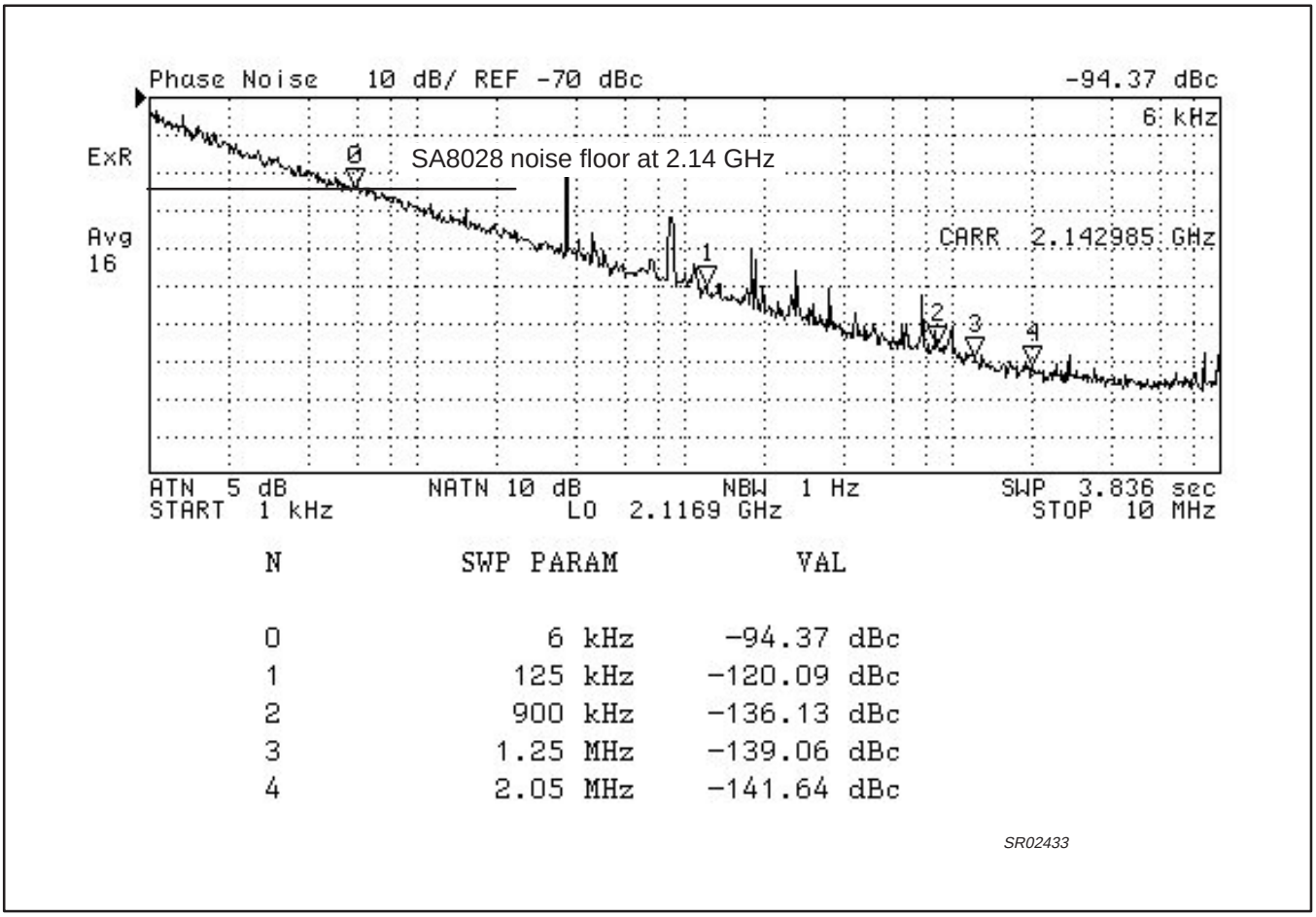


Figure 8. VCO Phase Noise plot for US-PCS band.

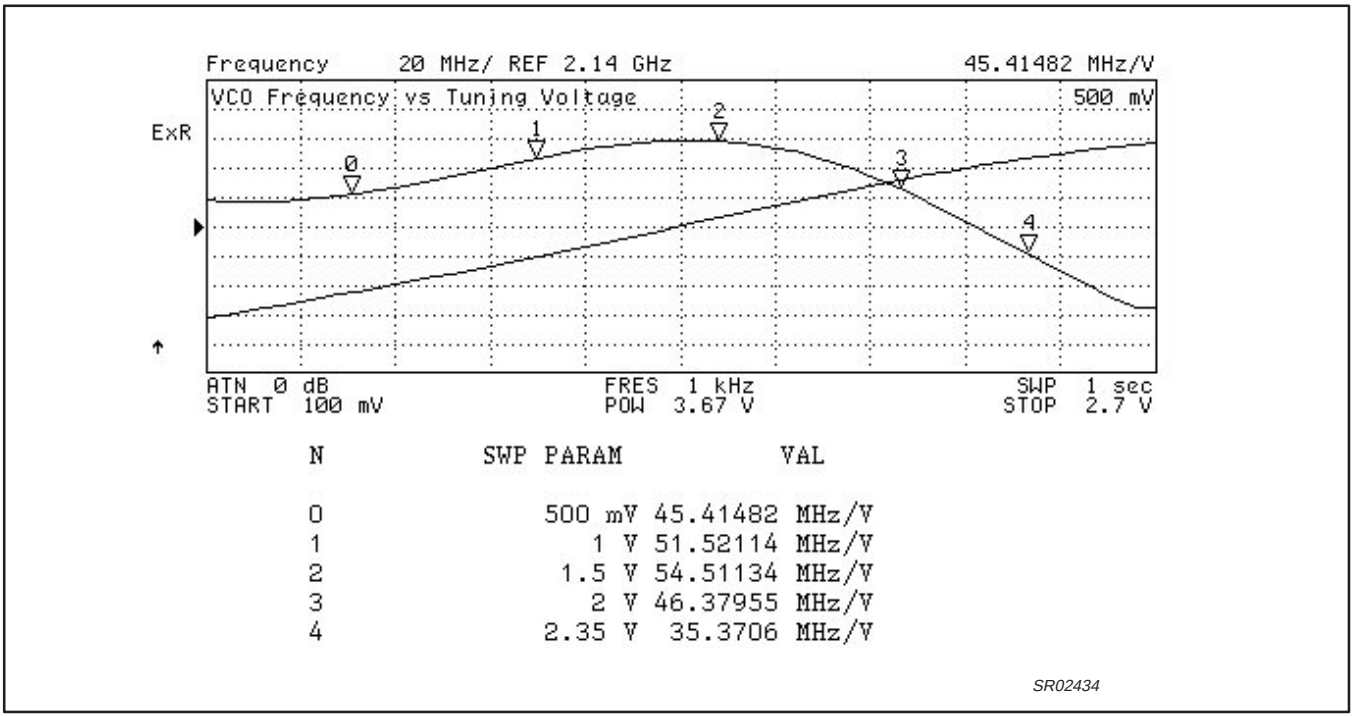


Figure 9. VCO tuning characteristics for US-PCS band.

Figure 9 illustrates that the tuning sensitivity of the VCO is approximately 50 MHz/V for the US-PCS band, which is beyond the needs of this application. However, this is quite reasonable when taking into account multiple IF frequency plans. The standard IF frequencies used today in mobile phone frequency plans is 85.38 MHz, 183.6 MHz and 210.38 MHz for both high-side and low-side injection. One other piece of data is the VCO tuning sensitivity for the CEL band. This was measured to be approximately 20 MHz/V.

Now that the VCO is chosen, a synthesizer that makes the most of the VCO's good characteristics must be found. This is done by utilizing the lowest in-band phase noise synthesizer available. By using such a synthesizer, the loop bandwidth can be reasonably wider; thus, reducing the PLL, frequency switching speed.

In determining the optimal synthesizer, the "normalized" synthesizer noise floor, *L(1 Hz)*, must be known. This is easily calculated, using equation 14, by knowing just a few parameters of a PLL with the synthesizer under test. First, with a wide loop bandwidth, approximately 60 to 100 kHz, measure the phase noise in the flat portion of the shoulder. This measurement is typically taken at 10 to 20 kHz away from the VCO frequency, as some of the close-in noise may be caused by the reference oscillator. Next, the FPD frequency and the feedback divider value, N, must be known. For this example, the SA8028 at 984 MHz, FPD frequency of 19.68 MHz and N equal to 50, the in-band phase noise was measured to be –101 dBc/Hz@20 kHz, +/–2 dB.

$$L(1Hz) = (-101\frac{dBc}{Hz}) - 20 \times \log(n) - 10 \times \log(f_{PFD}) \quad (14)$$

$$= (-101\frac{dBc}{Hz}) - 20 \times \log(50) - 10 \times \log(19.68e+6) = -208\frac{dBc}{Hz}, +/-3dB$$

Once the normalized noise floor is calculated, calculate the phase noise at the desired band frequency with the PFD frequency to be used. For Figure 7, the optimal loop bandwidth is where the following calculated in-band phase noise crosses the phase noise of the VCO.

$$L(f) = (-208\frac{dBc}{Hz}) + 20 \times \log(N) + 10 \times \log(f_{PFD})$$

$$= (-208\frac{dBc}{Hz}) + 20 \times \log(54) + 10 \times \log(19.68e+6) = -100.4\frac{dBc}{Hz}$$

The –100.6 dBc/Hz in Figure 7, is at approximately 7 kHz. By going through the same exercise for the US-PCS band VCO data yields a bandwidth of approximately 6 kHz.

Once these values are known, the loop filter can be calculated using equations 8 through 13 in Section 1.1.4. It's worth noting that the most rigid requirement to meet is the AMPS Intermodulation Spurious Response requirement. Therefore, when designing the loop filter, it is recommended that the initial design be done for the CDMA requirements using the charge pump gain mode of 3xIset. When the system goes into the AMPS mode, switch the charge pump gain mode to 1xIset. This reduces the loop bandwidth by approximately 1.7. This feature is illustrated in Figures 12 through 16.

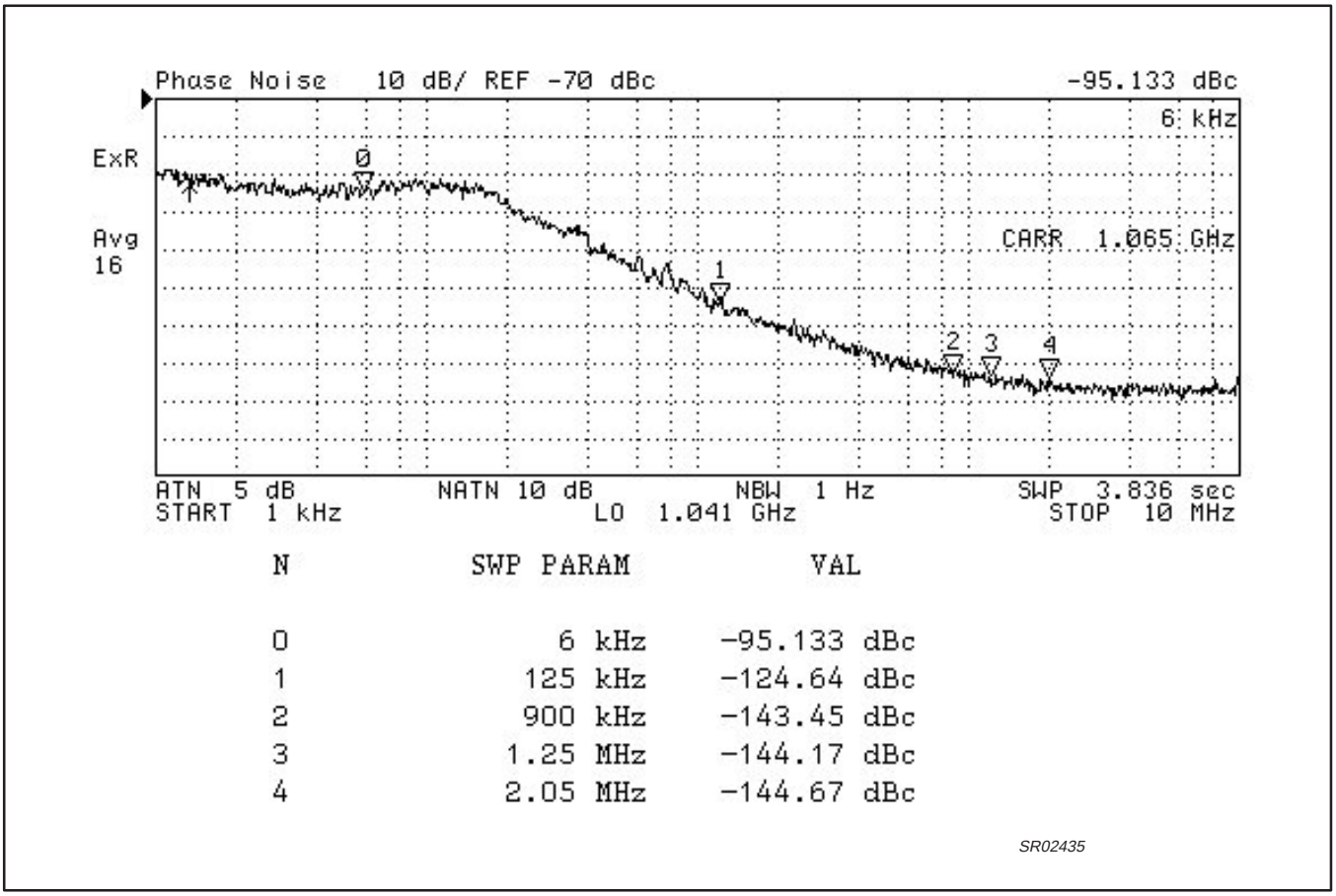


Figure 10. PLL Phase Noise Plot for CEL band CDMA standard.

Figure 10 illustrates the closed loop phase noise for CDMA in the CEL band with a damping factor of 0.99. This is confirmed by the low peaking at the loops natural frequency. For damping factors much smaller than 1.0, the integrated phase error is increased due to the peaking at the corner frequency. With the same loop filter, the PLL phase noise plot in the PCS band looks like that shown in Figure 11. It is acceptable to use the same loop filter because the ratio between the N_{CEL} and N_{PCS} is approximately 1/2. Furthermore, the ratio between $Kvco_{CEL}$ and $Kvco_{PCS}$ is also approximately 1/2. Therefore, the differences in equation 8 (N and Kvco), Section 1.1.4, between the CEL band and PCS band have minimal effect on loop stability.

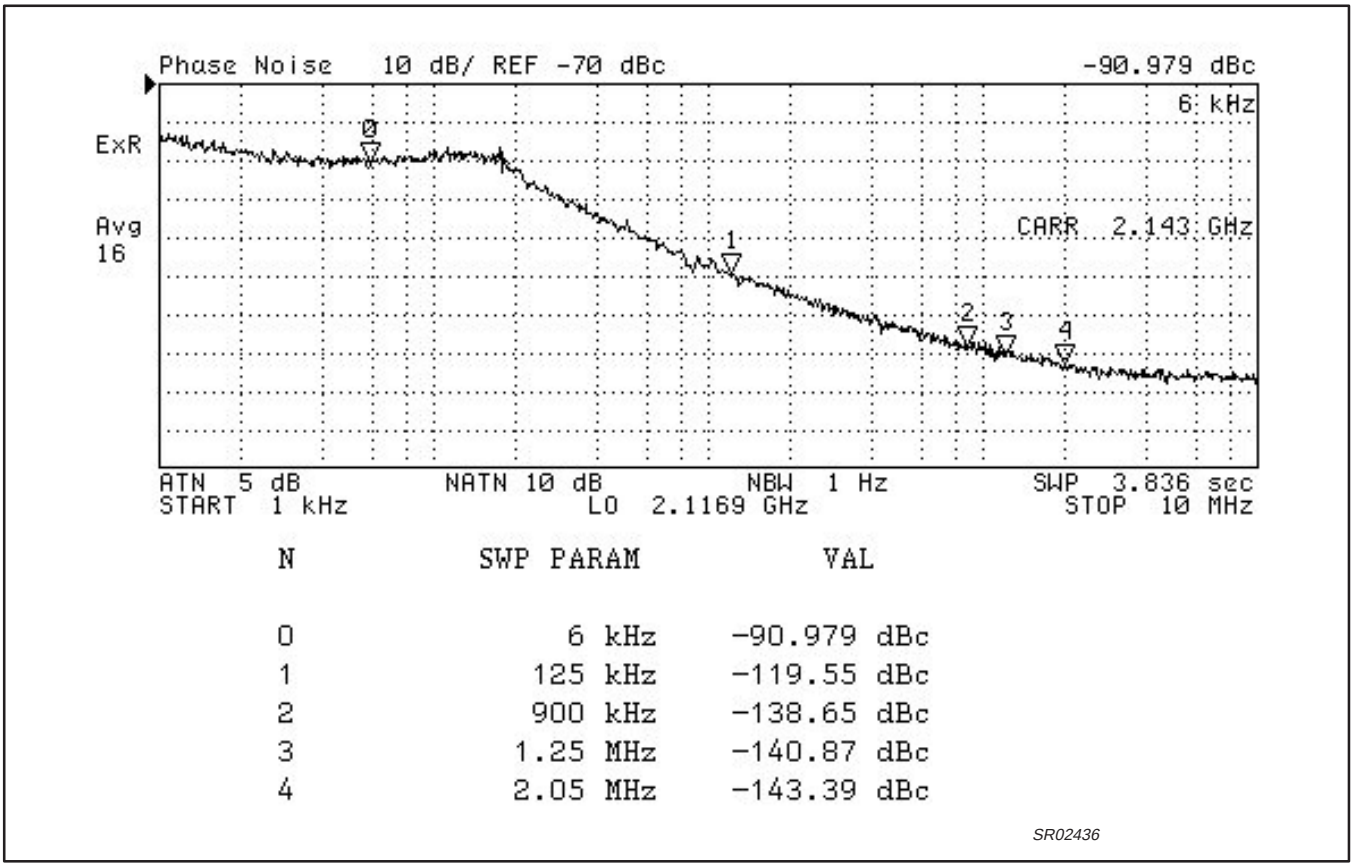


Figure 11. PLL Phase Noise Plot for PCS band CDMA standard.

In Figure 11, the loop bandwidth is slightly wider than in the case for the CEL band, this is due to the slight VCO gain difference; not quite a factor of 2.

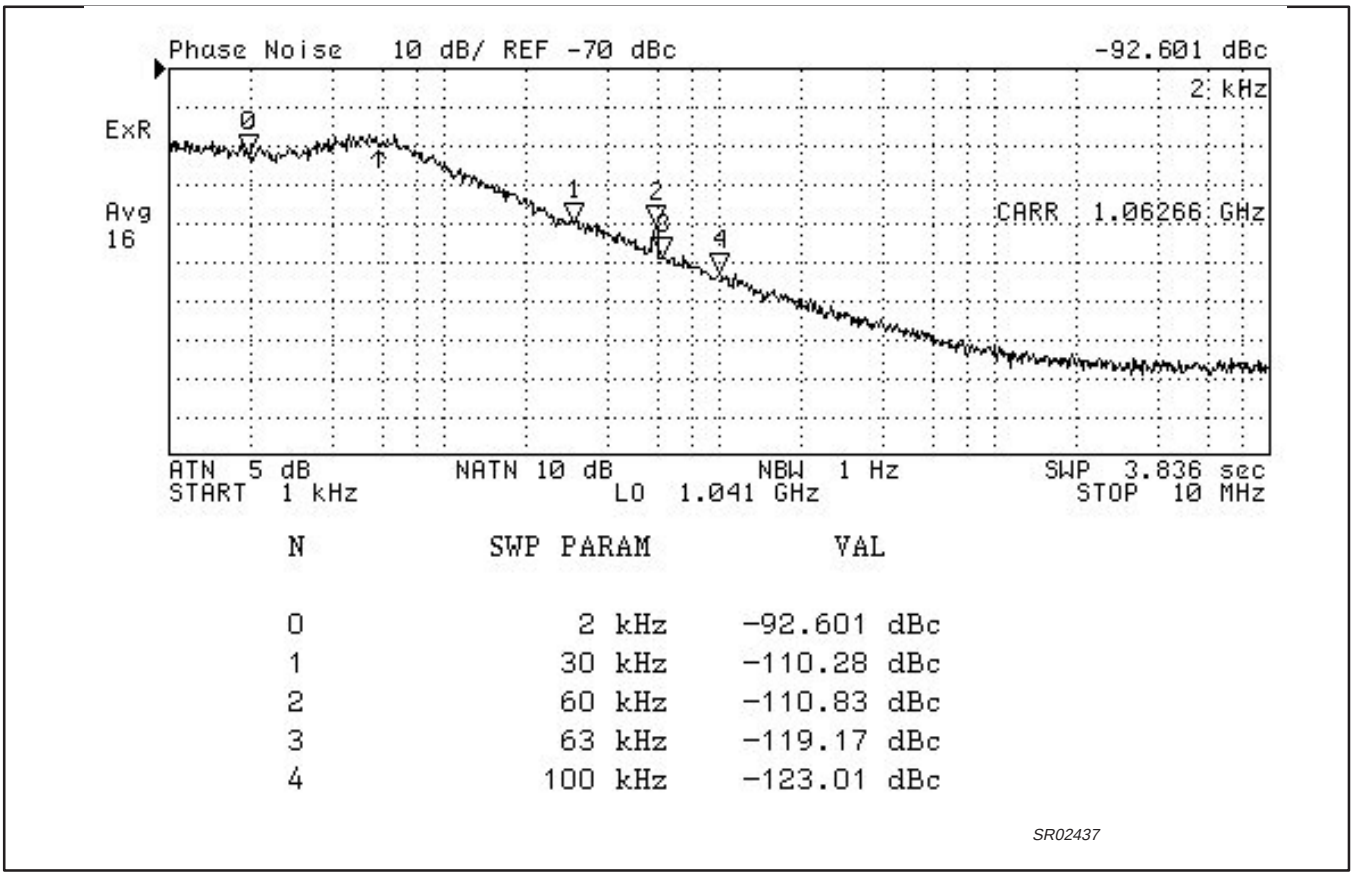


Figure 12. PLL Phase Noise Plot for AMPS mode (charge pump gain set for 1xIset).

Figure 12 demonstrates that the closed loop, natural frequency is reduced by approximately 1.7 times with the same loop filter and changing only the charge pump gain from 3xIset to 1xIset. This figure is not intended to show spur levels. The level shown here is misleading as some important information is missing. Figures 13 through 16 demonstrate the spurious improvement between the two charge pump modes, critical for switching from CDMA mode to AMPS mode.

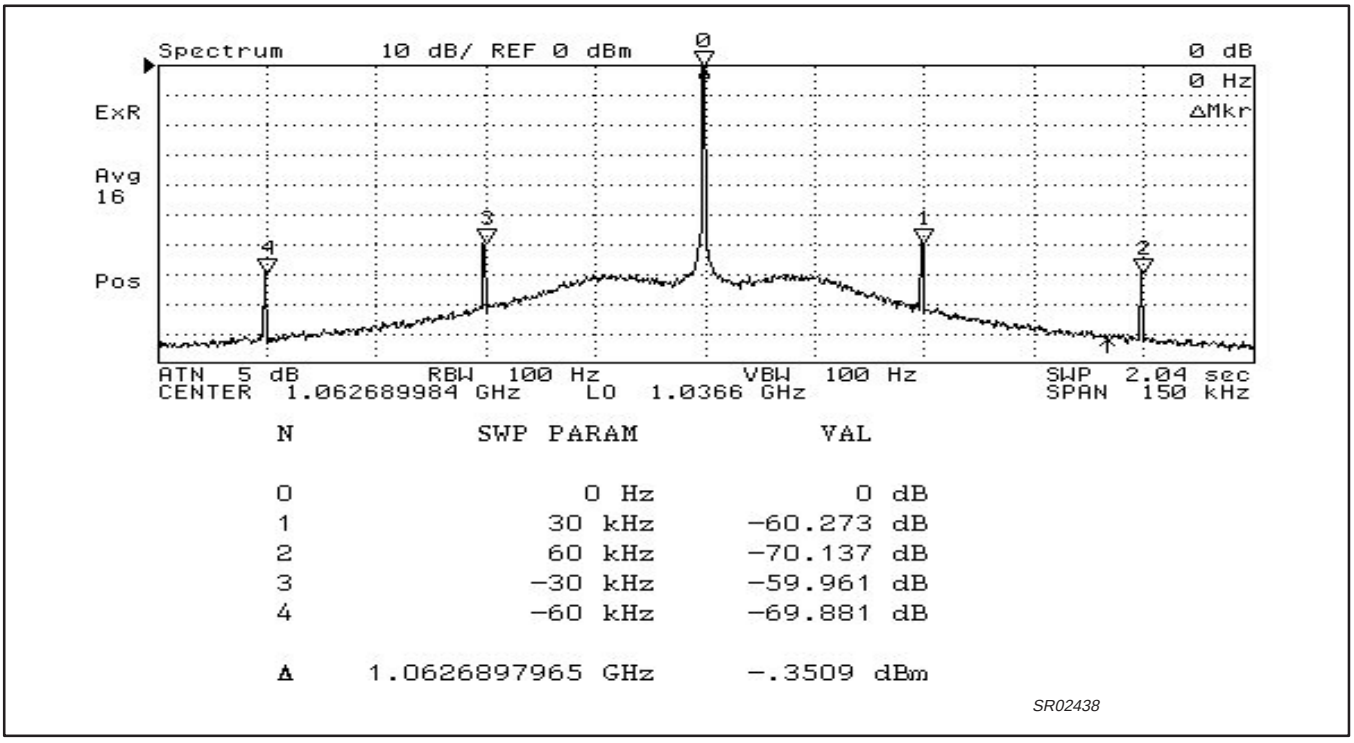


Figure 13. PLL 30 kHz Spurious Plot for AMPS mode (charge pump gain set for 3xIset).

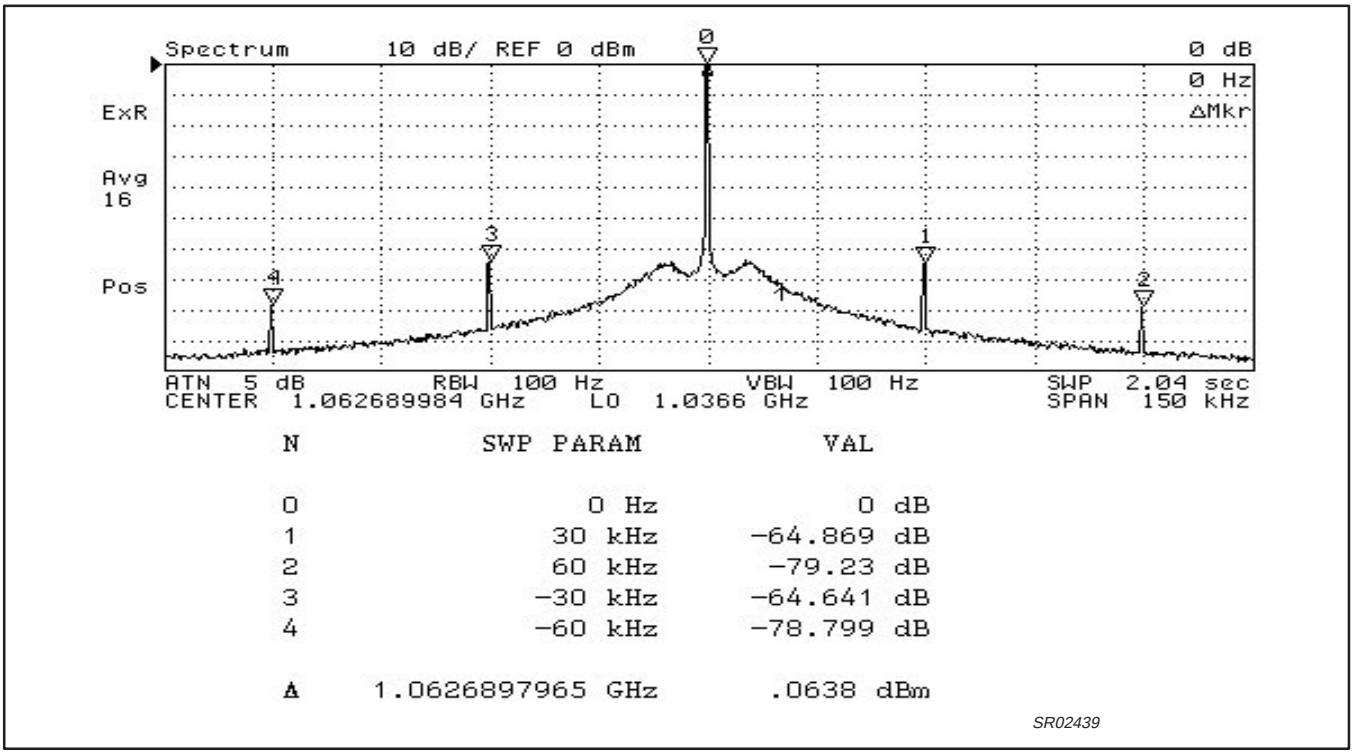


Figure 14. PLL 30 kHz Spurious Plot for AMPS mode (charge pump gain set for 1xIset).

The difference in spurious rejection is quite clear between Figures 13 and 14. The only change made to the loop was setting the charge pump gain from 3xIset to 1xIset via software. Figures 15 and 16 illustrate the same improvement in spurious rejection for the spurious located at 60 kHz offset.

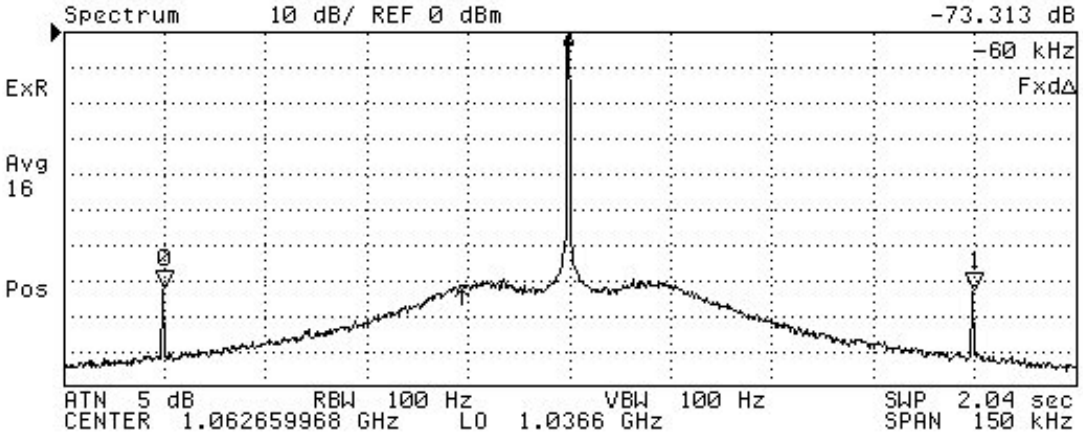


Figure 15. PLL 60 kHz Spurious Plot for AMPS mode (charge pump gain set for 3xIset).

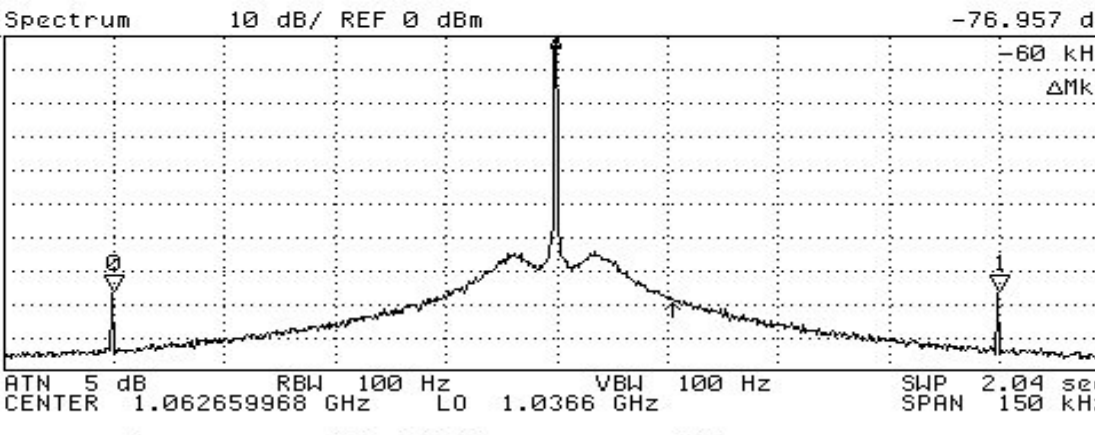


Figure 16. PLL 60 kHz Spurious Plot for AMPS mode (charge pump gain set for 1xIset).

MEASUREMENTS

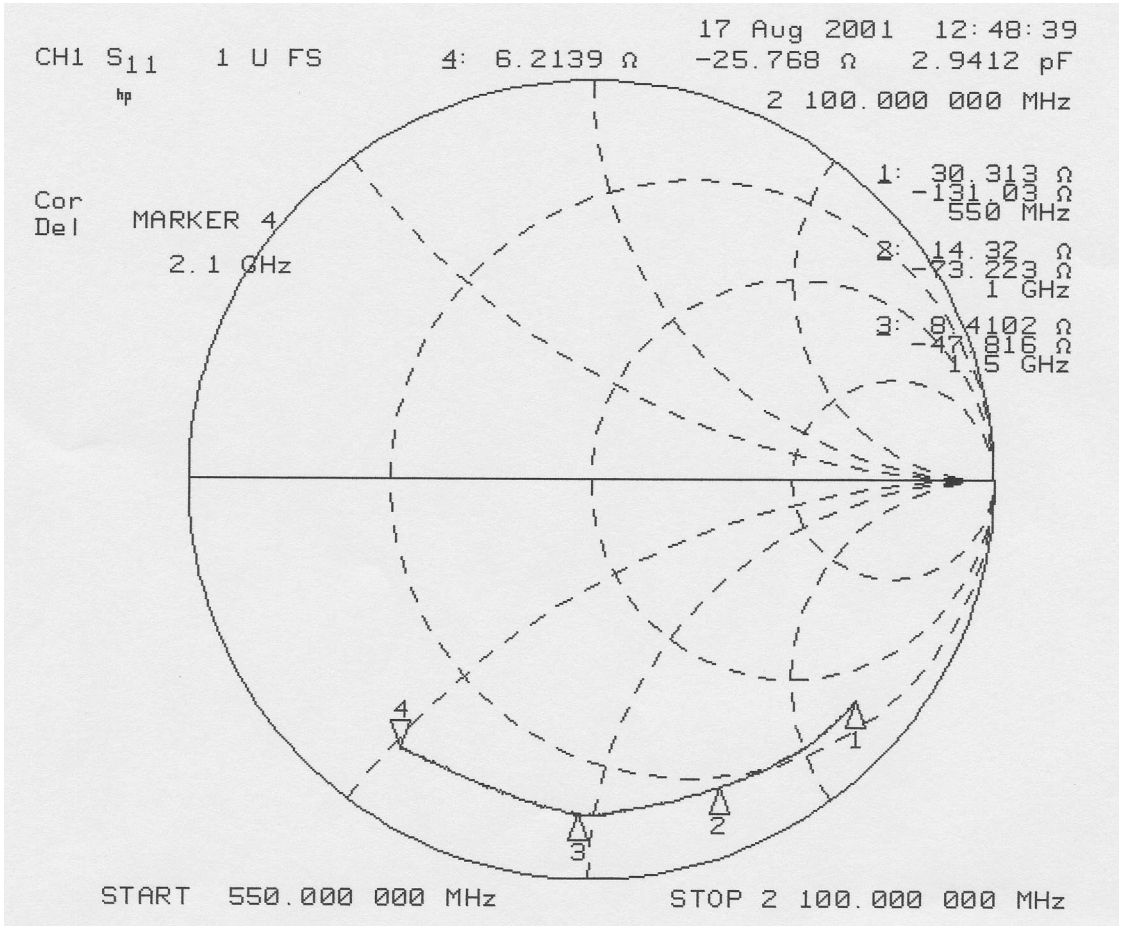


Figure 17. RFin+ Input Impedance.

Figure 17 is the measured input impedance to the RFin+ pin with a series 68 pF capacitor used as a DC blocker.

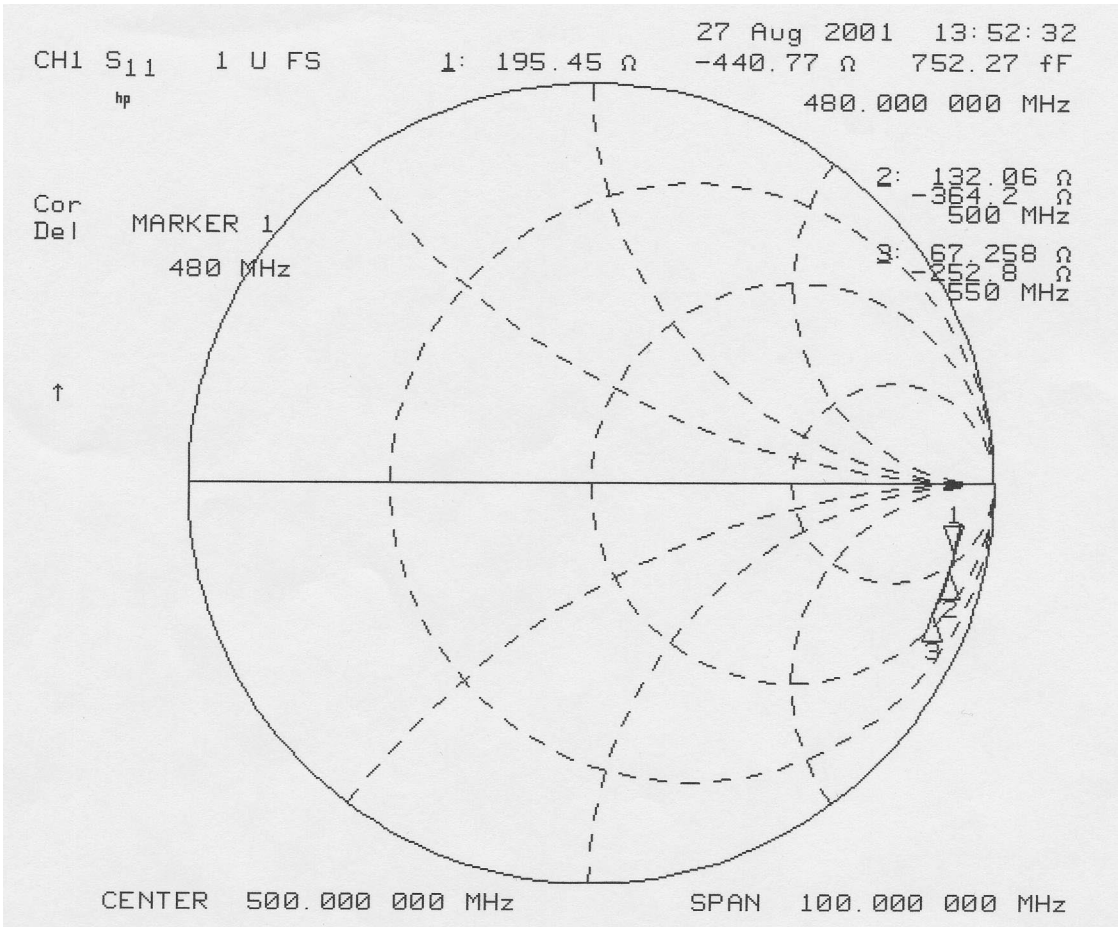


Figure 18. IF (Aux.) Input Impedance.

Figure 18 is the measured input impedance to the IFin (AUXin) pin with a series 330 pF capacitor used as a DC blocker.

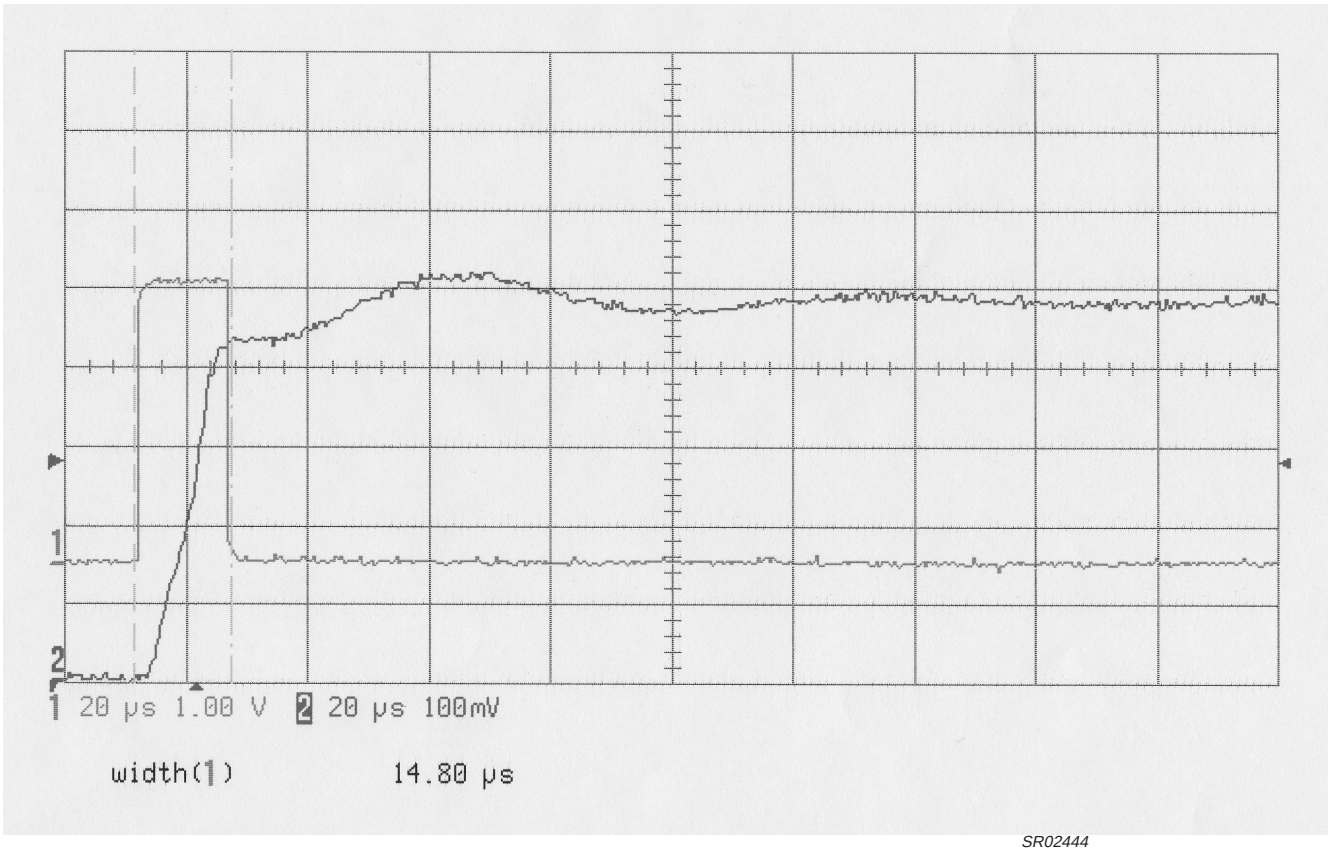


Figure 19. Strobe Pulse Width verses Loop Filter Charge Build-up.

Figure 19 illustrates what Section 1.1.2.1, Charge Pump Speed-up Mode, explains. The short pulse, trace 1, is the strobe pulse. In this case, the pulse is high for only 14.80 µS. The strobe pulse width will vary depending on the total, loop filter capacitance. Notice that the overshoot and ringing of the loop filter transient, trace 2, is minimized. With less overshoot and ringing, the total switching time between VCO states is reduced. The charge pump gain mode used to measure Figure 19 was CP1 = 0 and CP0 = 0, in speed-up mode. The loop filter configuration can be seen in Figure 4 of Section 1.1.2.

QUESTIONS AND ANSWERS

Q There is no reference divider for the RF path. How do I set the phase detector to my desired channel spacing?

A As the SA8028 is a high modulus fractional synthesizer and there is no reference divider. The phase detector frequency will be the same frequency present at the REFin pin. To program the channel frequency, follow the procedure described in Section 1.2.3, RF (Main) Divider.

Q I've noticed some "walking spurs" (dynamic spurs) on the spectrum analyzer when the span set in the 100 kHz range. However, these spurs are not very noticeable when the span in on the order of 10 kHz. What causes these spurs?

A These spurs are a type of "fractional spur". However, they are randomized by the sigma-delta calculator. The magnitude of these spurs very depending on the amount of VCO modulation by the VC-TCXO, or reference signal. This can happen in many ways. Therefore, care must be taken to minimize this effect when designing and laying-out the PLL. It has been observed in the lab that minimizing the Vtune line length between the synthesizer and VCO helps significantly, as does isolating the VC-TCXO. Another suggestion is to minimize the series resistance in the loop filter, the Vtune line will have a pulse signal on the order of 50 pS for a 20 MHz reference frequency.

Q What will happen if the strobe pulse width is wider than the loop filter capacitance charge time?

A Keep in mind that the speed-up mode changes the entire PLL characteristics. The intent of the speed-up mode is to rapidly set Vtune for the VCO. Effectively, the speed-up mode can be considered an open loop function. Therefore, when the strobe pulse goes low, the loop will close. If the strobe pulse width is too wide, the actual signal acquisition is undesirably delayed.

Q I've tested our design for AMPS Intermodulation Spurious Response requirements. The spurious levels from the synthesizer have caused the system to fail. How can I improve the spurious performance?

A As the SA8028 is a fractional synthesizer, there will be spectral splatter due to the phase detector output modulation. However, the magnitude of the spurs can be minimized by using just a few simple techniques. Since the signal from the charge pump is at the same frequency as the phase detector, which is the same as the reference input signal, care must be taken when designing and laying-out the PLL. This is done by minimizing the possibility of modulating the Vtune line to the VCO by keeping the Vtune line length at a minimum and keeping the series resistor of the loop filter small. It is also important to know the VCO coupling and what the effective input resistance is, at the phase detector frequency. Another area of susceptibility is the DC supply to the synthesizer. Care must also be taken to minimize the noise on the VDD, VDDpre, and particularly the VDDcp supply lines. If there is still concern about the magnitude of the spurs for the AMPS mode, use the 1xIset charge pump mode. It is recommended that the loop filter be designed using the 3xIset mode, as explained in Section 2.0. By programming the charge pump gain to 1xIset, the loop filter bandwidth is reduced by approximately 30%.

LIST OF REFERENCES

"*AN1893; SA8028/7026/8016/7016 Low voltage Fractional-N dual frequency synthesizers",* dated 1999 Nov 16, Philips Semiconductors

2.5 GHz Σ–Δ Fractional-N RF / 760 MHz Integer IF Synthesizer

AN10140

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